

Dr.R.SAKTHIVEL,Ph.D.,Sr.MIEEE,

1005, Rajeswari Towers, VIT Quarters, Vellore-632014, TN, India

Mobile No- +919994627570; 7010610583

E-mail: rsakthivel@vit.ac.in; dhillsakthi@gmail.com;

http://orcid.org/0000-0002-1879-2080

Scopus Author ID 55247470400



Dr.SAKTHIVEL RAMACHANDRAN (Senior Member, IEEE) received his bachelor's degree in electrical engineering from Madras University, in 2000, the Master degree in applied electronics from Anna University, in 2004, and the Ph.D. degree in the area of low-power high-speed architecture development for signal processing and cryptography. He is currently working as an Associate Professor with the School of Electronics Engineering, Vellore Institute of Technology, Vellore, India.

He is a co-author of the book "Basic Electrical Engineering published by Sonaversity, 2001 and the author of the "VLSI Design" published by S. Chand in 2007. He has published more than 60 peer reviewed papers in international conferences/journals. He has delivered around 50 guest lectures/invited talk and hands on workshop in the area of FPGA-based system design, full custom IC design, RTL to GDSII and ASIC Design.

His research interests include low-power VLSI design, developing high-speed architectures for cryptography and image processing. His current research interests include Neuromorphic computing and making efficient hardware for AI and ML.

He was heading the VLSI division at VIT, Vellore, India since 2009 to 2012. During his tenure he was instrumental in setting up SoC Design Lab, FPGA/ASIC Lab, Analog IC Design Lab in association with Cadence, Altera and Texas Instruments (India) Respectively.

He was a consultant/corporate trainer for Texas Instruments (Banglore), BOSCH (Banglore& Coimbatore), Pantech Solution(Chennai) and Wipro(Banglore). Prior to joining academia, he was the co-founder for the company Silicon to chip Technologies, Salem, India. He has mentored 30 undergraduate, 60 Post graduate students, 9 PhD students (3 finished PhDs), and 1 M.Tech (Research).

ACADEMIC QUALIFICATIONS

- **DOCTOR OF PHILOSOPHY (PhD) (2009-2014)**

University : School of Electronics Engineering, VIT University.

- **MASTER OF ENGINEERING (2002-2004)**

Institution : GCT, Coimbatore, Anna University

- **BACHELOR OF ENGINEERING (1996-2000)**

Discipline : Electrical and Electronics Engineering (EEE)

APPOINTMENTS HELD

IN ASSESSMENT AND ACCREDITATION PROCESS

- ✓ *Trained ISO Auditor*
- ✓ *Internal Auditor in IQAC at VIT*
- ✓ *ABET Accreditation coordinator at my Division as Division leader in 2012.*

ACADEMICS & MANAGING

Sl.No	College/Company	Position	Duration	Years
1.	VIT University	Programme Manager (M.Tech-VLSI) Division Leader-VLSI Division	2009-2012	3Yrs
		Project Coordinator	2012	1
		Class Coordinator (M.Tech-VLSI)	2014	1
		ABET Accreditation Coordinator	2012	1

INDUSTRY & CONSULTANCY

Sl.No	College/Company	Position	Duration	Years/Month
1.	Silicon To Chip Technology, Salem	Junior Design Engineer	25/12/2003 to 1/7/2004)	7 Months
2.	Texas Instruments	Consultant	2/5/2011 to 31/6/2011	2 Months
3.	Pantech Solution(Chennai)	Consultant		
4.	KARMIC, Banglore	Training	2/5/2011 to 31/6/2011	2 Months
5.	BOSCH(Banglore & Coimbatore)	Training		

BOOKS PUBLISHED

- 1) R.Sakthivel, M.Sathyanarayanan and Sivagamy "**Basic Electrical Engineering**"
Published by Sonaversity in the year 2001.
- 2) R.Sakthivel, "**VLSI DESIGN**", Published by S.Chand and Co., Delhi in 2000
- 3) R.Sakthivel, J.Jayagowri "**Digital IC Design with Timing Issues**", PHI publications in press

HONOURS AND AWARDS

- ✚ Co-Author for developing the "Technology Vision-2035" from TIFAC, DST India

- ✚ Won second prize for *Medical Hackthon conducted in VIT in association with Harvard University* for the topic “Development of Nano Electronic Wireless Belt (NEWB).
- ✚ Interviewed as “The Featured person” by Texas Instruments in the UniTi Newsletter Nov 2011. <http://www.uniti.in/component/content/article/82>
- ✚ Runner up for the Cadence Design Contest 2011 on the Topic “An efficient VLSI architecture for variable threshold simple edge preserved de-noising technique algorithm with improved signal to noise ratio”
- ✚ "A Novel Low-Power Area Efficient Reconfigurable Pipelined Two's Complement Multiplier with Reduced Error" Received *third prize* in WIPRO Paper presentation AAROHAN-2009
- ✚ *Fellowship Award for VLSI DESIGN-2008 Conference held in Hyderabad.*
- ✚ Received the *Research award from VIT University* for the last 7 years.

TRAINING PROGRAM CONDUCTED / INVITED TALK DELIVERED

- Conducted around *45 workshops in the area of VLSI* in different colleges in south India
- Delivered more than *25 invited talks all over south india*

REVIEWER FOR INTERNATIONAL JOURNAL

- 1) Reviewer for Elsevier Microelectronics Journal
- 2) Reviewer of IEEE Transactions on Circuits and Systems II
- 3) Reviewer of I4) Reviewer of Int. J. of Circuits and Architecture Design
- 5) Reviewer of IEEE Access

FUNDED PROJECT EXPERIENCE

<p>TITLE: A Scenario Analysis of Manufacturing Technologies for Electronic Appliances & ICT under Technology Vision 2035. J P Raina, Z C Alex and R Sakthivel</p>	<p>Duration: 07/2012- to date Sponsor: TIFAC/ DST, Govt. of India. Role : Co-PI</p>
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SEED MONEY FOR RESEARCH GRANT 2019 Title of the Project : High Performance ECC Processor Architecture Design for IoT Security Applications Faculty Details: Dr. Sakthivel R , Emp.Id: 10540	Amount sanctioned: 2.5 L Vellore Institute of Tecchnology (VIT), Vellore Department: School of electronics engineering, Micro and Nanoelectronics.
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INDUSTRY COLLABORATION

- 1. Lab Created:** “Texas Instruments Analog System Design Lab”, **Supported by:** Texas Instruments, Bangalore. **MoU Signed Dt:** 15/4/2011
- 2. Lab Created:** “Cadence Analog System Design Lab”, **Supported by:** Cadence, Bangalore. **MoU Signed Dt:** 29/06/2010.
- 3. Lab Created:** “FPGA/ SOPC Lab”, **Supported by:** Altera, Banglore, **MoU Signed Dt:** 13/3/2010

PUBLICATIONS

Published nearly 60 research papers in peered reviewed journals and international conference

<http://orcid.org/0000-0002-1879-2080>

<https://www.scopus.com/authid/detail.uri?authorId=55247470400>

MY ONLINE VIDEOS

<https://www.youtube.com/watch?v=2F5SkYbJVw0>

<https://www.youtube.com/watch?v=3IL--LULJEg>